REMARKS

Claims 1-15 were previously pending. By the foregoing amendment, claims 1, 3-5, 7, 8, 10, and 13 have been amended. No new matter has been added. . The amendments are fully supported by at least Fig. 3 and the written description on page 6 of the present application. Thus, claims 1-15 are currently pending and subject to examination.

Claims Rejections - 35 U.S.C. § 102 and 103

Claims 1 and 7–8 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Asai et al. (US 6,222,980). Claims 2–6 and 9–15 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Asai et al. It is noted that claims 1, 3-5, 7, 8, 10, and 13 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicant respectfully traverses these rejections as follows.

Claim 1 is directed to a method for decoding a Linear Time Code (LTC) frame of the type used in connection with film and television and accompanying audio, including in part, detecting a valid synchronization sequence within an incoming LTC frame **while** measuring a predetermined symbol interval relative to a reference clock including

> triggering a half-symbol duration counter upon a first change in a bi-phase mark symbol;
>
> upon a second change of the bi-phase mark symbol, stopping the half-symbol duration counter, storing a current count, and resetting the half-symbol duration counter;
>
> counting the half-symbol duration until a third change of the bi-phase mark symbol; and
>
> comparing the current count to a previously stored count to determine whether the synchronization sequence is valid.

Claim 1 has been amended to clarify the manner in which a valid synchronization sequence is detected "while" measuring a predetermined symbol interval relative to a reference clock. Claims 8 and 13 include similar subject matter.

As described on page 5, lines 27-29 of the present application, "proper operation [of the LTC receiver] . . . depends on its ability to change states in synchronism with the bi-phase mark transitions within an incoming LTC frame." The method in amended claim 1 provides the ability to detect " a valid bi-phase mark sync sequence while simultaneously measuring the current frame's half symbol interval," as described on page 3, lines 19-20 of the present application.

The Applicant notes that the method enables decoding LTC bi-phase-mark encoded data streams over any combination of operating conditions including (1) forward and reverse stream directions, (2) bit symbol rates from X/30 to 80*X, where X is the nominal LTC frame rate, and true and complement data polarity. *See*, e.g. page 13, lines 23-27 of the present application. In addition, because of the bi-phase mark modulation method, the polarity of the transition of the first bit of the synchronization word may differ from LTC frame to LTC frame depending on the number of logical zeros in the data. An LTC receiver/method according to the present application is capable of decoding streams of either true or complement polarity. *See*, e.g. page 14, lines 4-7 of the present application. Further, this digital implementation is capable of operating with a high-speed clock that can be asynchronous to the LTC bit symbol rate. *See*, e.g. page 14, lines 8-10 of the present application.

As previously noted by the Applicant, Asai deals with pulse widths, or symbol intervals, separately from the detection of a synchronization sequence. Asai specifically requires that the pulse width be addressed prior to the synchronization symbol because Asai uses the pulse width to determine the value of each bit. *See*, Asai column 11, lines 59-65 and Fig. 9, blocks 303-309. Asai needs the previously determined pulse width information in order to determine where the sync word begins and ends. *See*, Asai Fig. 10 blocks 315-335. Asai specifically illustrates that the step of measuring the pulse width occurs in steps 302 and 304 prior to blocks 312 and 324 dealing with sync words. Column 7, lines 1-22 of Asai merely describe the basic aspects of a standard LTC signal, and column 7, lines 40-65 describes where Asai finds pulse width information in response to a direction signal.

Asai does not count a half symbol duration based upon changes in a bi-phase mark, and does not compare a current half symbol count to a previously stored count in order to determine whether the synchronization sequence is valid, as in claim 1.

For at least this combination of reasons, the Applicant submits that Asai fails to disclose or suggest all of the subject matter of amended claim 1, and likewise amended claims 8 and 13.

Thus, claims 1, 8, and 13 are allowable over the cited art. As claims 1, 8, and 13 are allowable, the Applicant submits that claims 2-7 and 9-12, and 14-15, which depend from allowable claims 1, 8, and 13 are therefore also allowable for at least the above noted reason and for the additional subject matter recited therein.

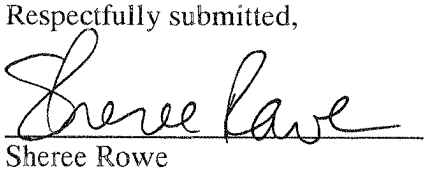
Further, with respect to claim 13, the Applicant notes that the LTC receiver includes three separate counters, and a state machine that is responsive to the three separate counters. In the Advisory Action, only the first counter is addressed. The Applicant submits that even if Asai "determines whether or not 80 bits in the memory have been accessed," Asai fails to disclose or suggest an LTC receiver having three separate counters, as described in claim 13, and fails to disclose or suggest a state machine responsive to the counts of the three separate counters, as in claim 13.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-15 in the application are patentable. Accordingly, reconsideration and allowance of this application are earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

In the event that any fees are due with respect to this paper, please charge Deposit Account No. 01-2300, referencing Atty. Docket No. 033163-00920.

Respectfully submitted,



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